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10/645,501	08/22/2003	David Peyton Cox	200206848-1	8776

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INTELLECTUAL PROPERTY ADMINISTRATION  
FORT COLLINS, CO 80527-2400

EXAMINER
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ZHEN, LI B

ART UNIT	PAPER NUMBER
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2194

NOTIFICATION DATE	DELIVERY MODE
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08/11/2008

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/645,501	COX, DAVID PEYTON	
	<b>Examiner</b>	<b>Art Unit</b>	
	Li B. Zhen	2194	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 23 May 2008.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

1. Claims 1 – 28 are pending in the application.
2. In view of the Appeal Brief filed on 5/23/2008, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.  
To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

### ***Response to Arguments***

3. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**5. Claims 6, 7, 13 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 7,222,348 to Athreya et al. [hereinafter Athreya].**

6. As to claim 6, Athreya teaches a method used while assembling in processor memory a stack of device objects (DOs) representing a device [device stack of the drivers for the device; col. 7, lines 8 – 25], the operating system of the processor having a kernel [col. 6, lines 8 – 25], the device having a corresponding physical device object [col. 7, lines 8 – 25], the method comprising:

determining a uni-role first driver registered to the device [device objects correspond to physical devices having M device types; col. 2, lines 20 – 30];

invoking the first driver, which includes passing the PDO of the device to the first driver [filter add device function 450 creates and initializes a new filter device object for the corresponding physical device object; col. 7, lines 8 – 25]; and

passing the PDO from the first driver to the multi-role second driver or to a component of the kernel [driver entry 410 provides an entry point for the UMD 220 in response to an IRP issued by the higher level driver 218; col. 6, lines 60 – 67].

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7. As to claim 7, Athreya teaches a method used while assembling in processor memory a stack of device objects (DOs) representing a device [device stack of the drivers for the device; col. 7, lines 8 – 25], the device having a corresponding physical device object (PDO) [col. 7, lines 8 – 25], the method comprising:

determining a driver registered to the device [device objects correspond to physical devices having M device types; col. 2, lines 20 – 30];

invoking the driver, which includes passing the PDO of the device to the driver [filter add device function 450 creates and initializes a new filter device object for the corresponding physical device object; col. 7, lines 8 – 25]; and

passing the PDO away from the driver without attempting to attach to the stack a DO corresponding to the driver [driver entry 410 includes a driver object pointer 415 that provides address reference or points to the major function group 420; col. 6, lines 60 – 67].

8. As to claim 13, Athreya teaches a method used while assembling in processor memory a stack of device objects (DOs) representing a device [device stack of the drivers for the device; col. 7, lines 8 – 25], the method comprising:

providing a multi-role driver for a plurality of device types [universal multipath driver (UMD) 220; col. 6, line 55 – col. 7, line 10]; but

not registering, in the registry of the operating system, the multi-role driver as having a role in assembly of the stack [driver entry 410 provides an entry point for the

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UMD 220 in response to an IRP issued by the higher level driver 218; col. 6, line 55 – col. 7, line 10].

9. As to claim 14, Athreya teaches the multi-role driver is operable to run in the WINDOWS Driver Model environment [col. 6, lines 8 – 25].

***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. **Claims 1 – 5, 8 – 12 and 15 – 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Athreya in view of U.S. Patent No. 7,093,265 to Jantz et al. [hereinafter Jantz].**

12. As to claim 1, Athreya teaches a method used while building in processor memory a stack of device objects (DOs) representing a device [device stack of the drivers for the device; col. 7, lines 8 – 25], there being a multi-role driver for a plurality of roles at least one of which corresponds to the device [universal multipath driver (UMD) 220; col. 6, line 55 – col. 7, line 10], the method comprising:

registering a plurality of uni-role helper drivers so as to uniquely correspond to the plurality of roles, respectively [device objects correspond to physical devices having M device types; col. 2, lines 20 – 30];

indirectly specifying a corresponding one of the multiple roles of the multi-role driver by specifying the helper driver mapped thereto [driver entry 410 provides an entry point for the UMD 220 in response to an IRP issued by the higher level driver 218; col. 6, line 55 – col. 7, line 10]. Athreya does not teach each helper driver mapping uniquely to one of the multiple roles of the multi-role driver, respectively.

However, Jantz teaches a plurality of helper drivers [HBA drivers 16; col. 10, lines 12 – 20], each helper driver mapping uniquely to one of the multiple roles [multipath driver has knowledge of the virtual-to-physical associations or mapping definition 132 that defines the relational correspondence between the physical paths and the virtual paths; col. 13, line 62 – col. 14, line 6 and col. 2, lines 15 – 20] of the multi-role driver [multipath driver 14; col. 4, lines 37 – 50], respectively.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the invention of Athreya to incorporate the features of Jantz. One of ordinary skill in the art would have been motivated to make the combination because this provides a multipath driver has increased transparency to the operating system and application layer due to its relatively lower-level functional position in the driver stack [col. 3, lines 30 – 36 of Jantz].

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13. As to claim 8, Athreya as modified teaches a method used while assembling in processor memory a stack of device objects (DOs) representing a device [col. 7, lines 8 – 25 of Athreya], there being a multi-role driver for a plurality of roles at least one of which corresponds to the device [col. 6, line 55 – col. 7, line 10 of Athreya], the device having a corresponding physical device object (PDO) [col. 7, lines 8 – 25 of Athreya], the method comprising:

providing a plurality of DOPush functions [col. 6, lines 60 – 67 of Athreya] in a multi-role driver [col. 6, line 55 – col. 7, line 10 of Athreya];

loading the multi-role driver into the memory so as to arrange for each of the DOPush functions to be directly invokable by a code portion external [col. 13, line 62 – col. 14, line 6 and col. 2, lines 15 – 20 of Jantz] to the multi-role driver [driver entry 410 provides an entry point for the UMD 220 in response to an IRP issued by the higher level driver 218; col. 6, line 55 – col. 7, line 10 of Athreya]; and

invoking, externally to the multi-role driver, one of the DOPush functions, which includes passing the PDO of the device to the invoked DOPush function [driver entry 410 includes a driver object pointer 415 that provides address reference or points to the major function group 420; col. 6, lines 60 – 67 of Athreya].

14. As to claim 15, Athreya as modified teaches a code arrangement on a machine-readable medium execution of which facilitates assembling in processor memory a stack of device objects (DOs) representing a device [col. 7, lines 8 – 25 of Athreya], the machine-readable code arrangement comprising:



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a multi-role driver code portion which corresponds to the device [col. 6, line 55 – col. 7, line 10 of Athreya], the multi-role driver code portion having exported functions corresponding to the multiple roles of the multi-role driver code portion [device objects correspond to physical devices having M device types; col. 2, lines 20 – 30 of Athreya], respectively;

a plurality of helper driver code portions [device objects; col. 2, lines 20 – 30 of Athreya]; and

an installer code portion for registering [col. 8, lines 25 – 35 of Jantz] the plurality of helper driver code portions so as to uniquely map to the multiple roles [col. 13, line 62 – col. 14, line 6 and col. 2, lines 15 – 20 of Jantz], respectively;

each helper driver code portion being operable to receive a corresponding PDO [col. 7, lines 8 – 25 of Athreya] and pass the PDO to the multi-role driver code portion without attempting to attach to the stack a DO corresponding to the helper driver code portion [driver entry 410 includes a driver object pointer 415 that provides address reference or points to the major function group 420; col. 6, lines 60 – 67 of Athreya].

15. As to claim 20, Athreya as modified teaches an apparatus having memory in which is buildable a stack of device objects (DOs) representing a device attached to the apparatus [col. 7, lines 8 – 25 of Athreya], the apparatus comprising:

multi-role driver means [col. 6, line 55 – col. 7, line 10 of Athreya] for operating according to a plurality of roles [col. 2, lines 20 – 30 of Athreya];

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a plurality of helper driver means [col. 7, lines 8 – 25 of Athreya] registered so as to uniquely correspond to the plurality of roles [col. 13, line 62 – col. 14, line 6 and col. 2, lines 15 – 20 of Jantz], respectively, of the multi-role driver [col. 2, lines 20 – 30 of Athreya]; and

means for selectively invoking the multi-role driver according to one of the multiple roles via invoking the corresponding helper driver mapped thereto [driver entry 410 provides an entry point for the UMD 220 in response to an IRP issued by the higher level driver 218; col. 6, lines 60 – 67 of Athreya].

16. As to claim 24, this is a program product claim that corresponds to method claim 1; therefore, this claim is rejected for the same reasoning as applied to claim 1 above.

17. As to claim 2, Athreya teaches the multi-role driver and the helper drivers are operable to run in the WINDOWS Driver Model environment [col. 6, lines 8 – 25].

18. As to claim 3, Athreya teaches a role is determined according to a device type for which the multi-role driver is invoked and the extent of the stack at the point at which the multi-role driver is invoked [col. 6, lines 60 – 67].

19. As to claim 4, Athreya teaches each of the multiple roles in the multi-role driver has a corresponding DOPush function, each DOPush function having been made

available to be invoked by a code portion external to the multi-role driver [col. 6, lines 60 – 67].

20. As to claim 5, Athreya teaches each helper driver includes an AddDevice routine that invokes a corresponding DOPush function in the multi-role driver, or each helper driver points to the address of the corresponding DOPush function in the multi-role driver [col. 6, line 55 – col. 7, line 10].

21. As to claim 9, Athreya teaches the DOPush function is invoked externally by an AddDevice routine of a helper driver, or the PnP manager, if the helper driver does not have the AddDevice routine [col. 6, lines 8 – 25], after the PnP manager is pointed to the address of the DOPush function by the helper driver, the helper driver being registered uniquely for the role to which the DOPush function corresponds [col. 7, lines 8 – 25].

22. As to claim 10, Athreya teaches the multi-role driver is operable to run in the WINDOWS Driver Model environment [col. 6, lines 8 – 25].

23. As to claim 11, Athreya teaches registering neither the multi-role driver nor the DOPush functions in the registry of the operating system as having a role in assembly of a stack representing a device [col. 6, line 55 – col. 7, line 10].

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24. As to claim 12, Athreya teaches a role is determined according to a device type for which the multi-role driver is invoked and the extent of the stack at the point at which the multi-role driver is invoked [col. 6, lines 60 – 67].

25. As to claim 16, Athreya teaches the multi-driver code portion and the helper driver code portions are operable to run in the WINDOWS Driver Model environment [col. 6, lines 8 – 25].

26. As to claim 17, Athreya teaches a role is determined according to a device type for which the multi-role driver code portion is invoked and the extent of the stack at the point at which the multi-role driver code portion is invoked [col. 6, lines 60 – 67].

27. As to claim 18, Athreya teaches the exported functions are DOPush functions [col. 6, line 55 – col. 7, line 10].

28. As to claim 19, Athreya teaches each helper driver code portion includes an AddDevice routine code portion that invokes the corresponding DOPush function in the multi-role driver code portion, or each helper driver code portion is operable to point to the address of the corresponding DOPush function in the multi-role driver code portion [driver entry 410 provides an entry point for the UMD 220 in response to an IRP issued by the higher level driver 218; col. 6, lines 60 – 67 of Athreya].

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29. As to claims 21-23, these are apparatus claims that correspond to method claims 2-4; therefore, these claims are rejected for the same reasoning as applied to claims 2-4 above.

30. As to claims 25-28, these are program product claims that correspond to method claims 2-5; therefore, these claims are rejected for the same reasoning as applied to claims 2-5 above.

#### **CONTACT INFORMATION**

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Li B. Zhen whose telephone number is (571) 272-3768. The examiner can normally be reached on Mon - Fri, 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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